ACCELERATED GRAPHICS PORT FOR A MULTIPLE MEMORY CONTROLLER COMPUTER SYSTEM

Abstract of the Disclosure

An architecture for storing, addressing and retrieving graphics data from one of multiple memory controllers. In a first embodiment of the invention, one of the memory controllers having an accelerated graphics port (AGP) includes a set of registers defining a range of addresses handled by the memory controller that are preferably to be used for all AGP transactions. The AGP uses a graphics address remapping table (GART) for mapping memory. The GART includes page table entries having translation information to remap virtual addresses falling within the GART range to their corresponding physical addresses. In a second embodiment of the invention, a plurality of the memory controllers have an AGP, wherein each of the plurality of the memory controllers supplies a set of registers defining a range of addresses that is preferably used for AGP transactions. In a third embodiment of the invention, a plurality of memory controllers implemented on a single chip each contain an AGP and a set of configuration registers identifying a range of addresses that are preferably used for AGP transactions.

[S:\DOCS\EMN\EMN-7770.DOC
062601]
S:\DOCS\EMN\EMN-4134.DOC:sad
020904